15.8 CMOS-on-Plastic Technology using Sequential Laterally Solidified Silicon Thin-Film Transistors

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Manufacturers of small and medium sized TFT LCD displays are making increasing use of low-temperature polysilicon (LTPS) rather than amorphous silicon (a-Si) thin-film transistors. The higher performance of LTPS TFTs permits row and column driver circuits to be integrated directly on the display glass, reducing display module cost and shortening product development times. The conventional commercial method for crystallization of the a-Si precursor film into polysilicon is excimer laser annealing (ELA). However, the performance of LTPS TFTs made with ELA-processed material is limited by the highly defected polysilicon microstructure produced with ELA.

Sequential lateral solidification (SLS) has been introduced and commercialized as a laser crystallization method that can produce large-grain polysilicon films and even single-crystal regions [1,2,3]. SLS is fundamentally different from ELA because it uses a patterned beam to induce lateral crystallization of the melted silicon from seeds in the neighboring region melted in the previous laser pulse. The SLS process not only produces higher performance TFTs than ELA, but also has higher throughput and a wider process window.

Prior to our work, SLS crystallization of silicon had only been successfully applied on glass substrates. We recently reported material studies showing that SLS can also produce large-grain polysilicon on plastic substrates [4]. Here we report the performance of SLS TFTs and circuits fabricated directly on plastic.

The substrate is a 10µm layer of spin-on polyimide on a 4in diameter silicon support wafer. Our earlier material studies showed that SLS crystallization of silicon works successfully on free-standing polyimide films [4], but for the TFT and circuit results reported here we applied the polyimide to a support wafer so that all of the conventional TFT fabrication steps could be performed in a standard silicon IC fabrication facility with automated wafer handling. In this paper a low-temperature process is described, which has a maximum temperature of 300°C for compatibility with the polyimide film.

Automated probing and characterization was performed on more than 20,000 NMOS and PMOS TFTs. Transistor yields were close to 100%. Typical transfer characteristics of NMOS and PMOS transistors with L=10µm and W=100µm are shown in Figs. 15.8.1 and 15.8.2. The field-effect mobilities on these devices are μ_n=191cm^2/Vs and μ_p=45cm^2/Vs, and the threshold voltages are V_{tn}=+1.1V and V_{tp}=–13.9V. Our low NMOS threshold voltages are ideal for low-voltage CMOS operation, but our PMOS threshold voltages are typically about –10V, requiring higher supply voltages. High threshold voltages are common for PMOS LTPS TFTs with undoped channels like ours. A p-type threshold voltage adjustment implant is often required to reduce the threshold voltage, but we have not yet implemented this implantation step.

An Agilent 8753ES network analyzer and calibrated microwave probe head were used to measure the high frequency performance of the NMOS and PMOS transistors. Typical results for 2µm channel length devices are shown in Fig. 15.8.3. The unity-gain frequency f_t is the frequency where the current gain h_{21} passes through unity (0dB gain). For the NMOS device f_t=257MHz, and for the PMOS device f_t=184MHz. These are the highest unity-gain frequencies ever achieved for transistors directly fabricated on plastic, to the best of our knowledge.

CMOS and NMOS circuits were fabricated with channel lengths of 2, 5, and 10µm. Over 100 circuits were tested, and nearly all were fully functional. The highest performance was obtained from CMOS circuits with 2µm channel lengths, and we report those results here. Figure 15.8.4 shows results from a divide-by-two frequency divider operating at 10V. We found that the L=2µm CMOS frequency dividers are functional at 25MHz, though not at 50MHz, the next higher frequency available from our complementary clock generator. In Fig. 15.8.4 the output is measured with a probe that attenuates the voltage by 20:1, so that the input and output waveforms are on equivalent voltage scales, and have about the same voltage swing of 4-5V. Thus our divide-by-two circuits have large voltage swings, even at 25MHz.

Figure 15.8.5 shows a 2µm channel length five-stage CMOS ring oscillators functioning at 100MHz with a supply voltage of 15V. The peak-to-peak output voltage swing is only a few hundred millivolts because we deliberately made the ring oscillator output buffers small in order not to suffer yield loss due to large output buffer devices. However, this did not need to be a concern because of our high yields. The internal oscillator waveforms were measured using an active FET probe with an input capacitance of 40fF. The peak-to-peak internal voltage swings are 2.5-3.0V. To our knowledge, these are the fastest circuits ever built using transistors directly fabricated on plastic.

The results demonstrate that CMOS circuits using high-performance SLS silicon TFTs can be directly fabricated on plastic. NMOS devices with 2µm channel length have unity-gain frequencies of over 250MHz, and CMOS ring oscillators operate at 100MHz. Applications of the technology include flexible TFT displays and other flexible substrate applications, such as phased-array antennas, structural health monitoring arrays, and rugged digital X-ray imaging panels [5].

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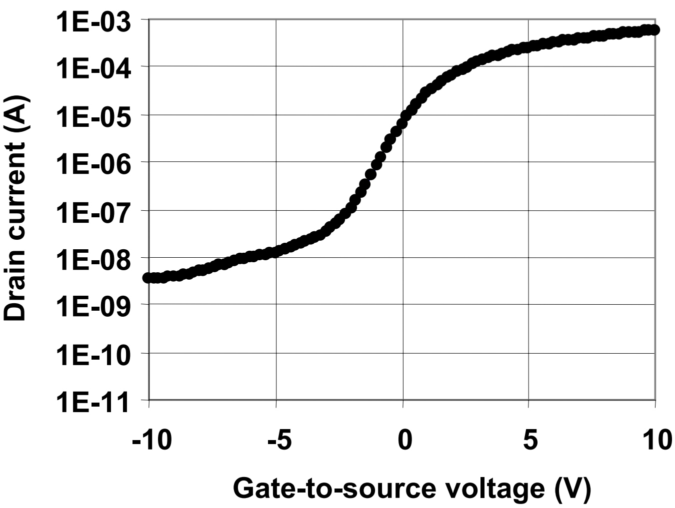

Figure 15.8.1: NMOS transfer characteristic.

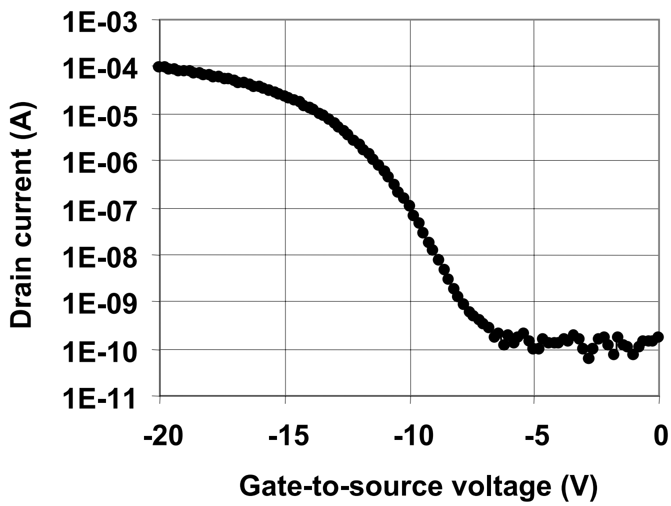

Figure 15.8.2: PMOS transfer characteristic.

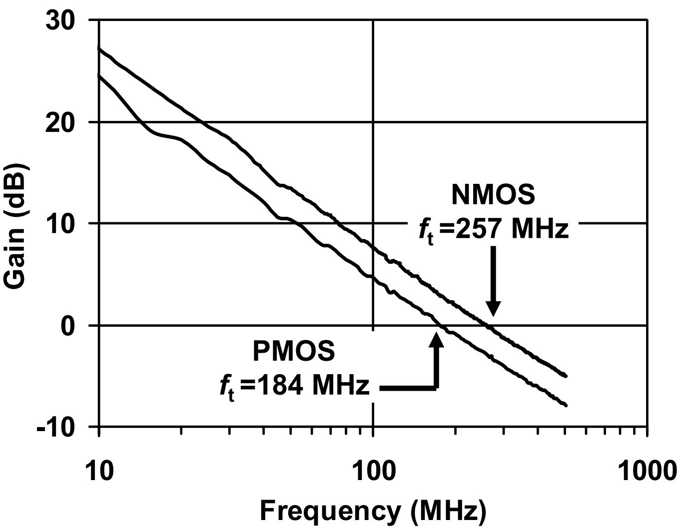

Figure 15.8.3: High-frequency characteristics of CMOS-on-plastic TFTs.

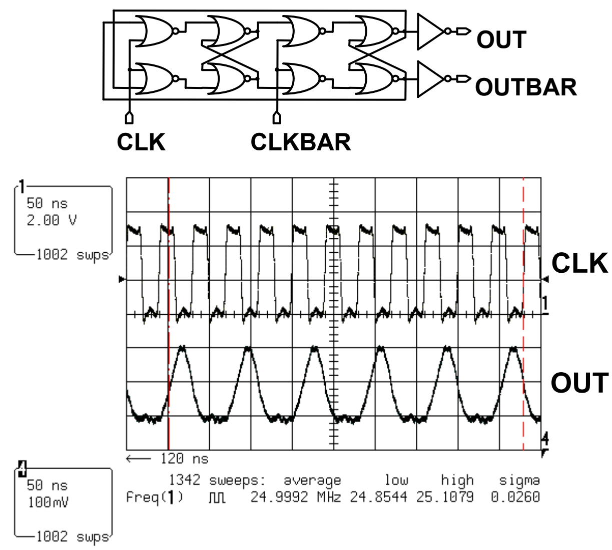

Figure 15.8.4: Logic diagram and 25MHz operation of CMOS frequency divider.

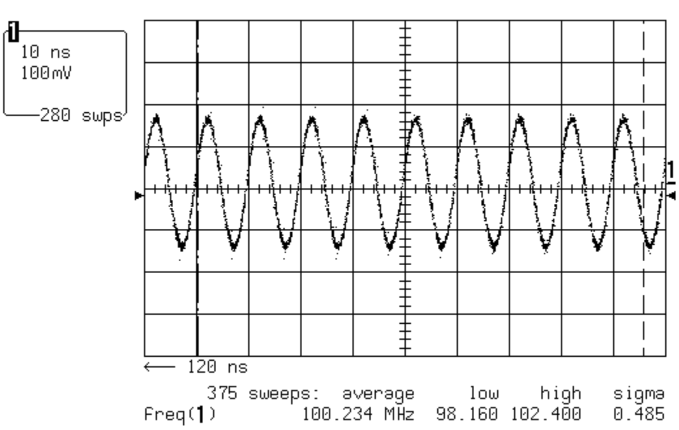

Figure 15.8.5: Five-stage CMOS ring oscillator operating at 100MHz.